e-Information on wires- A First Step towards 2-Terminal Silicon Nanowires for Electronic Memory Devices

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Abstract

Presently, there is a rapid growth of interest in the area of flexible electronics. Benefits such as light weight, durability and low-cost are among the most appealing aspects. However, the high temperatures throughout the fabrication processes are still the main hurdle.

In this study, the deposition of silicon nanowires (SiNWs) at low temperature (300˚C) using Tin (Sn) catalyst is studied. Silicon nanostructures have been the centre of research for many years for a number of applications in different areas. Chemical Vapour Deposition (CVD) and other industrial deposition techniques, for the growth of crystalline silicon micro- and nano-structures use high temperatures and therefore are not compatible with temperature sensitive substrates. This work utilises a low temperature deposition method for the growth of SiNWs and creates a leeway to use flexible plastic sheets as substrates. The silicon nanowires were deposited by exploiting the Vapour-Liquid-Solid (VLS) material growth mechanism using Plasma Enhanced Chemical Vapour Deposition (PECVD) technique.

The suitability of these structures, as an information storage material, for future flash and two terminals non-volatile memory devices are investigated. Strong charge storage behaviour with a retention time up to 5 hours was observed showing great potential for the future memory candidate.

Keywords: Silicon nanowires, electronic memory devices, PECVD, low temperature, VLS growth, quantum tunnelling, internal electric field.

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Introduction

Silicon nanowires (SiNWs) are one-dimensional nanostructures with numerous known applications, among them are biosensors [1], high performance field effect transistors [2] and solar cells [3]. The fabrication of silicon nanomaterials can be broadly divided into two approached : the top-down approaches (i.e. chemical and reactive-ion etching and nanolithography) and the bottom-up approaches (i.e. thermal evaporation, laser ablation and chemical vapour deposition). In the top-down technique the final device is created by etching away the unwanted material. Nanolithography techniques can be used to design certain geometrical shapes that result in desired nanostructures, nevertheless they are limited as this method is expensive with a low return.. The bottom-up method has a number of benefits of self assembly ability and no need for creating geometrical patterns since the desired structure(s) can be achieved by combining effectively fundamentals blocks.

The formation of single crystal SiNWs (that time called whiskers) by Vapour-Liquid-Solid (VLS) method was proposed by Wagner and Ellis in 1964. In their publication silicon crystal whiskers/wires with metal-liquid droplets at the tip were observed. Gold (Au) was the catalyst (or a seeding material) and a gas mixture of $SiCL_4$ and H_2 was used for the growth of silicon crystalline wire-type or whisker shaped structures [4]. It was proven that the metal catalyst is essential for the VLS growth. Till today these factors (Au, $SiCL_4$ and H_2) are the most common used for the VLS growth of nanomaterials. VLS can also be applied into different techniques for nanomaterials synthesis, such as evaporation oxide-assisted growth (OAG), Chemical Vapour Deposition (CVD), solution-phase synthesis, Molecular Beam Epitaxy (MBE) and thermal laser ablation [5]. Depending on the application, each technique can be chosen to obtained the desired material. The VLS growth method has a great advantage over other methods; it can produce geometrical structures well over a range of micrometres to nanometres. Following the path of VLS mechanism, a new field is emerging where alternative metals for catalyst-assisted silicon synthesis are investigated. Mainly because of the impurity of Au produces a deep defect level within the bandgap grown silicon structures and these defects effect both the electrical and optical properties of the structures grown. And, thus causing degradation in the electronic and optical devices [6].

In this work, the synthesis of SiNWs using Sn catalyst is carried out. For a relatively low temperature VLS growth of silicon nanostructures, Sn is a very promising alternative catalyst to gold. The Sn melting point (231.93˚C) is almost the same with the Sn-Si eutectic point (231.9˚C) [7]. As we know that the low eutectic point is one of the main criteria that encourages the growth of material of interest at low temperatures. The geometrical dimension of Silicon structures growth can be determined by the liquid alloy droplet size, the low silicon solubility of silicon in Sn and silicon concentration at the eutectic temperature.. Moreover, Sn introduces neutral impurity energy levels in the silicon bandgap [8] making it ideal for Si crystalline structures in electronic applications. While there are numerous publications regarding SiNWs growth using alternative metal catalysts, only a handful of preliminary studies have been reported for Sn-catalysed synthesis of SiNWs[9-11].

In the last two decades, flash electronic memory information storage technology has been playing a foremost role in the semiconductor industry. The extraordinary decrease in size of the electronic memory cell has led to smaller and everyday devices such as mobile phones, handheld computer and tablets [12, 13]. The increase in the use of the aforementioned electronic devices has led to the need of a memory that can cope with the new requirements of consumer electronics devices. Until now, there has been a general consensus among the electronic memory community [14, 15] that memories are chosen based on their application.

A new approach to scale the memory cell size down without compromising its performance is one of the indispensable requirements.

For further scaling down the size of the flash memory-type (using similar concept) devices, some material synthesis challenges should be taken into consideration, such as the scaling down of the tunnelling dielectric thickness or a different dielectric material. The tunnelling dielectric layer should be thin to allow the electrical charges to tunnel through (for the writing, erasing processes) but, at the same time, must be thick enough to safeguard retention of information stored[16]. There are a number of factors which can affect the reliability of memory devices. And, defects in the dielectric layer are among the most common factors. Their presence can result in higher operating voltages and higher leakage currents, and more adversely can lead to failure of the device. Moreover a realistic value for the length of the channel has to be maintained, which impedes the further scaling down of the memory cell. Additionally, the high deposition temperatures and the high generated thermal energy (which dissipates into the environment) are not favouring the continuous scaling down to the memory cells. Because of the decrease of the size, higher operating voltages are required [17] that may cause undesirable phenomena. The objective is to keep the total amount of energy during a process at a minimum level. This requirement can be fulfilled with a short time growth process (few seconds) because the total energy is temperature-time dependent. New device architectures as well as materials are being studied in order to overcome aforementioned problems. Among them, charge trapping devices, like Silicon-Oxide-Nitride-Oxide-Silicon (SONOS), were presented as one of the possible solutions. SONOS devices are utilising the intrinsic defects of the silicon nitride that can trap charges giving them the advantage of a simpler structure compare to flash memory devices [16]. Another idea (introduced in 1995 by Tiwari [18]) is to use metal or silicon nanocrystals for the floating gate. For the dielectric, high-k materials are primarily studied because of their great robustness to defects [19]. The barrier of the minimum channel length could be solved by three dimensional (3D) approaches because a multi level cell with the memory arrays vertically stacked is obtainable [17]. From another perspective totally new storage mechanisms are considered, such as the ferroelectric and phase change memories [20, 21]. Nevertheless, there are concerns about their reliability, besides their cost is higher compare to flash memory.

The high fabrication temperatures are the major challenges for flexible electronics. For plastic and flexible substrates a fabrication temperature of no more than 350˚C is generally acceptable. In the present study, Plasma Enhanced Chemical Vapour Deposition (PECVD) technique is chosen to overcome the thermal restrictions. The plasma activation has the advantage of reducing the deposition temperature from a range of 600-700˚C to 400˚C or even less [22]. In addition, this deposition technique has other benefits such as processing compatibility, which makes it possible to use the same method for the deposition of the gate dielectric as well as the active layers, minimising the process steps.

This article is reporting the fabrication and demonstration of a non-volatile memory device produced at 300˚C on glass substrate. This memory has the potential to develop into a flexible flash memory cell.

Materials and Methods

1. **Silicon nanowires growth:** The parameters presented in Table 1 were examined aiming to grow crystalline silicon nanostructures at a low temperature for non-volatile memory device applications. The substrate temperature and the metal catalyst, among other parameters used during the PECVD process, have a drastic effect on the growth of the silicon structures. Sn layers were deposited on glass (for Raman spectroscopy analysis) and on p-Si/SiO_2 substrates (for SEM analysis) in vacuum by thermal

evaporation. The silicon (Si) substrate has a native barrier layer of SiO_2 layer (2-3 nm) in order to prevent possible diffusion of the metal into Si.

Table 1: The conditions used for the synthesis of crystalline silicon nanowires; the thermal evaporation of catalyst material and the PECVD parameters.

Thermal evaporation of catalyst layer	Vacuum	1.5×10^{-6} mbar
	Deposition rate of Sn	0.5 nm/sec
PECVD conditions	RF Power	25 W
	Pressure	200 mTorr
	Gases	SiH_4 20 sccm H_2 100 sccm
	Substrate temperature	300˚C

Sn layers of 6 and 20 nm thickness were placed in the PECVD reactor and once high vacuum was ensured, the process started with the conditions presented in Table 1. Subsequently increasing the temperature to the required value, the system was left for five transactions to stabilise. Then H_2 plasma was activated for five minutes and later SiH_4 gas was added for five minutes. The whole growth process was performed in H_2 ambient. Here, we should point out the importance of the H_2 plasma. The existence of the hydrogen plasma step is fundamental. This treatment reduces the oxidised surface of the metal and assists the formation of catalyst droplets, which enhances the nanowire growth chances[23].

2. Fabrication of memory device

Only PECVD and thermal evaporation are utilised for the fabrication of the memory cell. This minimises the process complexity. Moreover, both techniques are compatible with conventional manufacturing systems. The silicon nanowires utilised for the memory element were prepared at 300˚C by the PECVD process as described earlier. A cross bar design with the silicon nanowires sandwiched between two insulating layers similar to an isolated floating gate was chosen. Aluminium top and bottom contacts of 200 nm thickness were thermally evaporated (with base pressure of 1×10^{-6} mbar) by Edwards Auto 306 evaporator. Silicon nitride thin films were deposited using the PECVD technique for the insulating layers, in particular, a tunnelling layer (30 nm) and a gate (blocking) dielectric (100 nm). For both, the insulating layers and the silicon nanowires a 13.56 MHz RF PECVD reactor was used.

3. Electrical characterisation of the memory devices

The most frequently used reliability parameters regarding the performance of electronic memory devices are the retention time and write/erase cycle endurance. In order to examine the retention time or the read stability over time of a device, a read voltage is kept applying immediately after the programming (positive voltage) or after the erasing (negative voltage). The response of current or capacitance is monitored as a function of time or number of read pulses. This study is very important for memory devices since immediately after the electrons are trapped, the stored electrons have a finite probability to tunnel back to the channel or substrate. Moreover, any random discharge can cause a gradual shift of the channel current or capacitance. Apart from outstanding memory retention time, fast programming, accessing and erasing are extremely desirable. Few years retention time may satisfy someone who needs an exceptionally fast flash memory. For testing a new device, a series of pulses are designed that program, erase and read the memory while the corresponding current is monitored. For accurate

measurements and reliable devices several hundreds of programming/erasing cycles should be performed.

Results and Discussion

This study is focused on two parts; the growth of silicon nanowires utilising low temperature fabrication techniques and the implementation of these structures as floating gate in memory devices.

1. Low temperature growth of silicon nanowires

For enabling the use of temperature-sensitive substrates, a metal with a low melting and eutectic point as well as a plasma-enhanced process was utilised in order to achieve a very low deposition temperature.

The following results have been obtained using Sn catalyst material for VLS growth by PECVD technique at low temperature (300˚C). The only drawback of the plasma-enhanced process is the simultaneous parasitic deposition of amorphous silicon, which in some cases can be dominant [24]. Henceforth, the crystallinity of the obtained nanostructures should be examined.

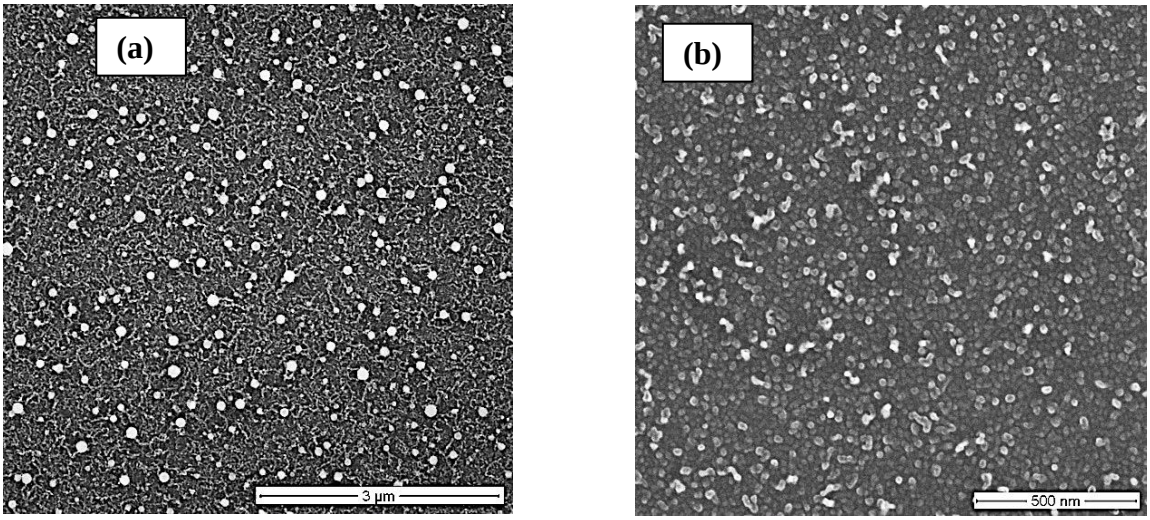
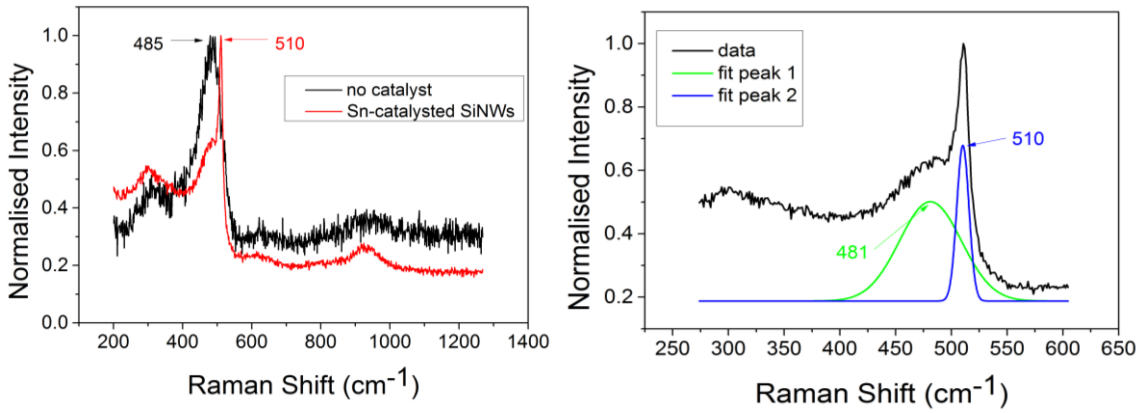


Figure 1 (a) Scanning Electron Microscope image of Sn (5nm)-catalysed SiNWs (b) SEM image of Sn (1nm)-catalysed silicon nanostructures. Both the structures grown by PECVD.

Figure 1 represents the SEM images after the PECVD process nanostructures from two different catalyst layer thicknesses. Nanowire growth was observed from an ultrathin layer of 1 nm Sn at 300˚C temperature. In both cases, the Sn catalyst was present on the tip of SiNWs in a spherical shape confirming VLS growth. The morphology and quality of the nanostructures depend on the growth conditions and the properties of the catalyst material.

Raman spectroscopy was performed in order to examine the crystallinity of the nanostructures fabricated in this study. Figure 2(a) shows the Raman spectra of the samples prepared in this work from Sn layer. The sharp peak at 510 cm^{-1} in the Raman spectrum proves that the nanowires are crystalline whereas the broad, amorphous silicon peak at around 485 cm^{-1} is detected when no catalyst layer was used and only an amorphous silicon film was deposited. The peak is noted to be slightly down shifted with respect to the bulk Si (519-520 cm^{-1}). This

shift is attributed to the small physical dimensions of the scattering crystals. The scattering of photons is affected by the diameter of nanowires resulting in a downshift of the Si peak and an asymmetric broadening [25, 26].



(a) (b)

Figure 2: (a) Raman spectrum of the silicon nanostructure sample grown via PECVD deposition from 6 nm Sn layer at 300 °C for 5 minutes. (b) Deconvolution of the first order Raman spectra shows the presence of a lower frequency peak in the range of 481-482 cm^{-1} corresponding to amorphous silicon.

A small shoulder on the left of the sharp peak (at around 510 cm^{-1}) of the crystalline silicon was noticed for a couple of Raman spectra. This signifies the parasitic deposition of amorphous Si. In order to examine the presence of any other peak, deconvolution of the spectra was realised as shown in Figure 3(b). These two peaks revealed that the SiNWs are crystalline (peak at 510 cm^{-1}) but amorphous silicon (peak at 481 cm^{-1}) is also present. It is worth mentioning that by conducting Raman analyses at several regions of the sample great homogeneity in the structure of the nanowires was found.

2. **Memory device characteristics:** The charging effect of the SiNWs is studied for their potential application as the storage component of non-volatile memory devices. The proposed structure is similar to a floating gate containing SiNWs insulated with two different in size silicon nitride layers as shown in Figure 3(a). The working principle is based on the hypothesis that under a positive electric field charges will tunnel through the thin tunnelling layer and store at the SiNWs while the blocking (or gate) layer will retain the charges and prevents them from continuing tunnelling further. In order to investigate this concept, devices with and without SiNWs were studied to determine which samples would exhibit charging memory behaviour.

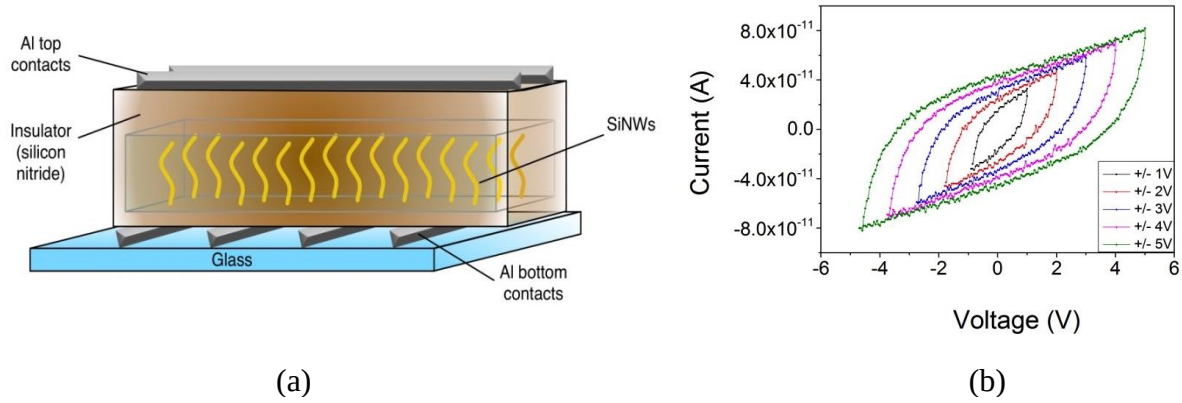


Figure 3: (a) Schematic of the proposed two-terminal non-volatile memory device. Silicon nitride dielectric layers insulate the SiNWs and there are aluminium top and bottom contacts. The entire memory cell is fabricated on glass substrate. (b) Current-Voltage (I-V) characteristics of the memory device using silicon nanowires for the storage element.

At first, Current-Voltage (I-V) measurements were carried out, where the current is monitored for negative and positive voltage sweeps, in order to determine if the I-V behaviour shows any hysteresis. Hysteresis loop observed by I-V and capacitance-voltage (C-V) measurements is an indication for charging and discharging procedures [27]. Figure 3(b) shows the I-V characteristics in which the voltage sweep starts from ± 1 V and goes up to ± 5 V. This hysteresis may originate memory behaviour, which may arise from the presence of defect states. In order to gain information about defect states, capacitance measurements were performed in which the capacitance is measured as a function of frequency or voltage at a constant temperature. To ensure the precision of the capacitance and to avoid it from being caused by other parasitic capacitances within the memory structure, a sample without SiNWs was also tested and compared to the memory device. The defect states of capacitors can be studied by performing Capacitance-Voltage-Frequency sweeps at a constant temperature. The defect states located in any interface region may form a continuous distribution of energy levels [28]. The frequency of the AC signal used in the C-V measurement is very crucial since it can determine the response time of the trap states. Traps near the band edge emit much quicker than deep traps in the bandgap. Hence, the deep level defects (or traps) respond to the low frequencies [8, 28].

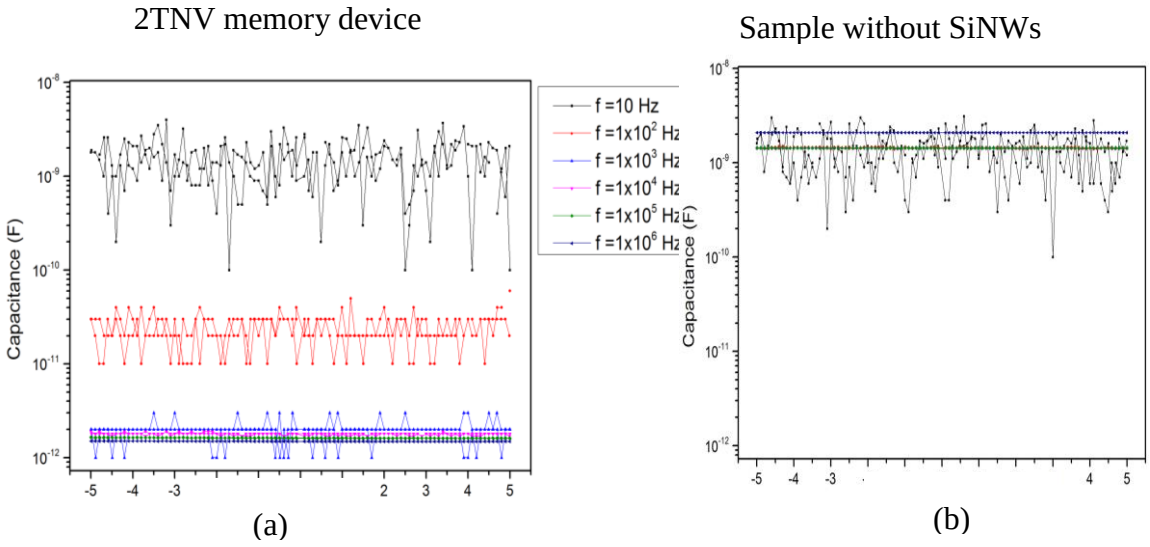
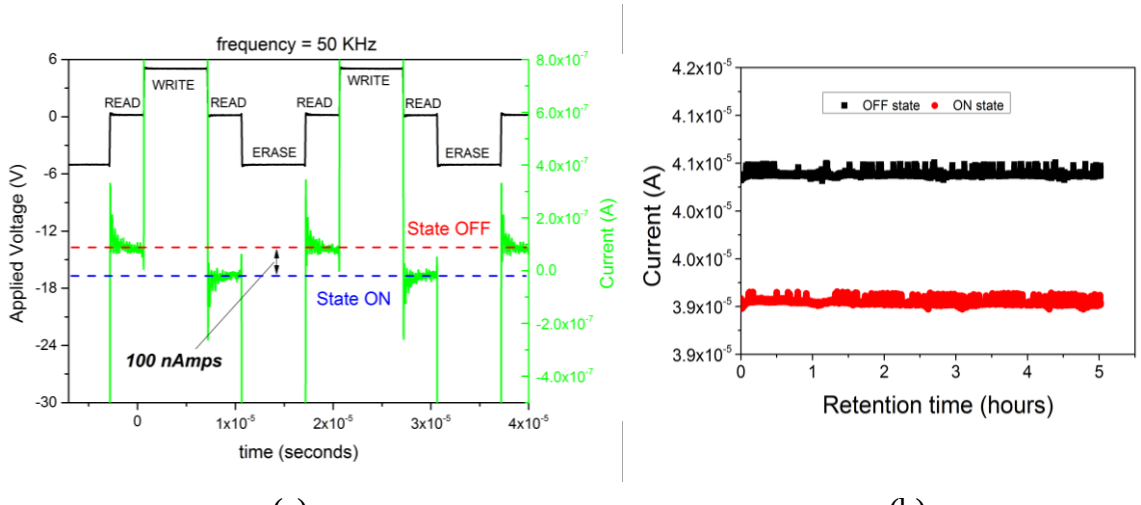


Figure 4: Capacitance-Voltage plots of the 2TNV memory device on glass(a) and without silicon nanowires(b). The frequency was varied from 10 Hz to 1 MHz for a ± 5 V sweep at room temperature. It is observed that for the

memory device the capacitance is inversely proportional to the applied frequency demonstrating an existence of deep defect states.

Figure 4 demonstrates the C-V sweep of the memory device and the reference sample (without SiNWs) for a wide range of frequencies. These results show that the capacitance of the memory cell depends on the measured frequency. In particular, as the frequency increases the capacitance was found to decrease indicating the existence of deep levels. Since the deep levels do not respond to small *ac* signal variation of the gate voltage, no capacitance is contributed at the higher frequency C-V [28]. This is verified here because the variation of the capacitance becomes smaller as frequency increases. This is also in agreement with the model presented by Zhu et al. [29] in which minor capacitance variation is observed. When increasing the frequency, the charge mobility becomes smaller and that leads to higher relaxation time. A higher relaxation time means that it is more difficult for the carriers to response to the *ac* signal hence a smaller variation of the capacitance is sensed. This model was created based on HfO_2 MIM capacitors but it can expand to other high-k materials.

A Write-Read-Erase-Read (W-R-E-R) voltage pulse was produced in order to further validate the electrical bistability of the novel memory devices. The operating voltages (write and erase) were selected to be lower than the breakdown voltage of the insulators in order to ensure no physical damage was done to the devices during the repeatable cycles. Also, the read voltage was selected to be low enough not to enhance the probability of the tunnelling phenomena but just to monitor the state.



(a) (b)

Figure 5: (a) The W-R-E-R voltage cycle (black line) and the current output of the memory (green line) at a frequency of 50 kHz. Write and erase voltages of ± 5 V amplitude and + 0.2 V for read voltage. During the read pulse two different states are observed (ON and OFF) with a difference in current of around 100 nA. (b) Data retention characteristics of the memory on glass containing SiNWs.

As it was expected, during the read process two different states were observed. After writing at + 5 V, the memory showed a low conductivity (State ON) while after erasing a high conductivity (State OFF) is observed (Figure 5(a)). Two different states were measured during the read process with a 100 nA current difference. Moreover, this behaviour was proven to be repeatable over time for countless cycles. Hence, it shows that the proposed memory device undergoes a transition between two states (ON and OFF), which is maintained over time.

Another important factor of a memory is the time that it can retain the information for. For that reason, data retention time measurements were conducted where the two states are monitored over time. In particular, a pulse/function generator (HP/Agilent 5116A 50 MHz) was programmed to apply + 5 V write, - 5 V erase pulses and AC current bias of 20 mV for read signal at 1 MHz. An output resistor (300 Ω) was connected in series to the memory. The output was measured with a microprocessor digital voltammeter (Solartron 7055 Schumberger). Figure 5(b) represents the retention time characteristics of the non-volatile memory device. Once writing (or programming) the memory device, state ON was observed while after the erase process, state OFF was noted with a different current value. The two states are very discrete and the device was stable for 15,000 reading pulses and 5 hours retention time was monitored. The value of an AC current measurement is higher than of DC measurements. This is due to decrease in the device impedance as we increase the frequency. Both DC and pulsed-DC measurement show reversal current and it can be explained, as pictorially presented in Fig-7, on the basis of the internal electric field.

3. Principle of device operation

The working mechanism of the novel non-volatile memory device presented in this paper is discussed here. The memory effect of the memory device is attributed to the storage behaviour of the SiNWs. The energy band diagrams of the memory at equilibrium and programming are presented in Figure 6. The proposed working mechanism of the non-volatile memory cell with SiNWs as the floating gate is based on the creation of an internal electric field and its exploitation to create bistability in electrical conductivity.

When a high voltage is applied across the device (Vwrite > 0) there is a high probability that the electrons will tunnel through the insulator and get trapped in the storage medium (in this case: the SiNWs). As soon as a lower but still positive external filed (Vread < Vwrite) is applied, a huge decrease in the current response is observed. During the read process, the effective voltage across the device is less than the applied voltage due to the formation of a negative internal electric field (E_i). The measured negative current value shows that Ei is higher and opposite in direction to the electric field (E_o). The observation of low conductivity could correspond to state ‘0’ of a memory bit. Once the same amplitude voltage in the opposite direction is applied (Verase = -Vwrite) the tunnelling phenomena will once again dominate and the electrons will tunnel away from the medium. When the read process is performed once more after the erase step, the direction of E_i changes and a high current state is monitored (named state ‘1’). This leads to the conclusion that the SiNWs get charged and form an internal electric field. The direction of this internal field can either augment or oppose to the total external electric field. This is reflected in the I-V hysteresis and is depicted as electrical bistability.

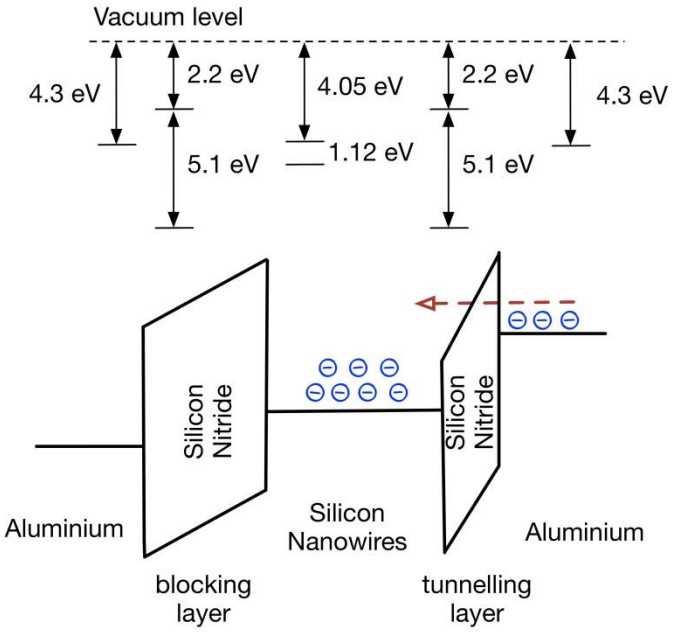


Figure 6: Energy band diagrams and illustration of programming process of the non-volatile memory device.

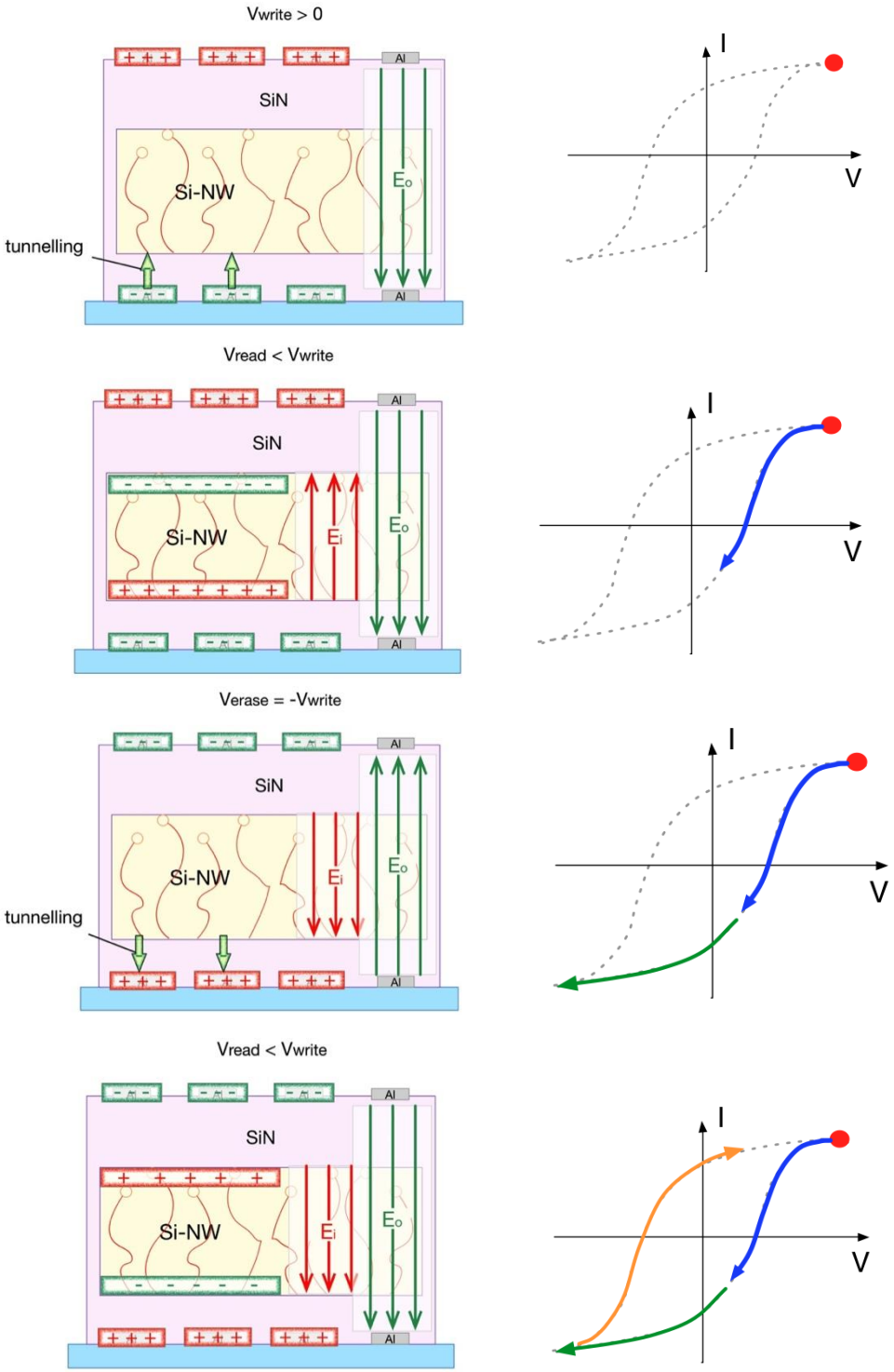


Figure Error! No text of specified style in document.**: Schematic illustration demonstrating the working mechanism of the proposed 2TNV memory device during the write, erase and read process with the corresponding current-voltage (I-V) plot.**

Conclusions

It is found that Sn-catalysed crystalline SiNWs can be synthesized successfully at 300°C. The Raman spectra showed a narrow peak representing the crystalline structure of the SiNWs. It was discovered that only 6 nm of the Sn layer is needed to initiate the SiNWs growth with the specific set of PECVD conditions used in this work. Moreover, memory effect attributed to the presence of SiNWs was proven. The electrical characterisation of the samples revealed that the novel memory devices can be rewritten many thousands of times and demonstrated a retention time of up to 5 hours.

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